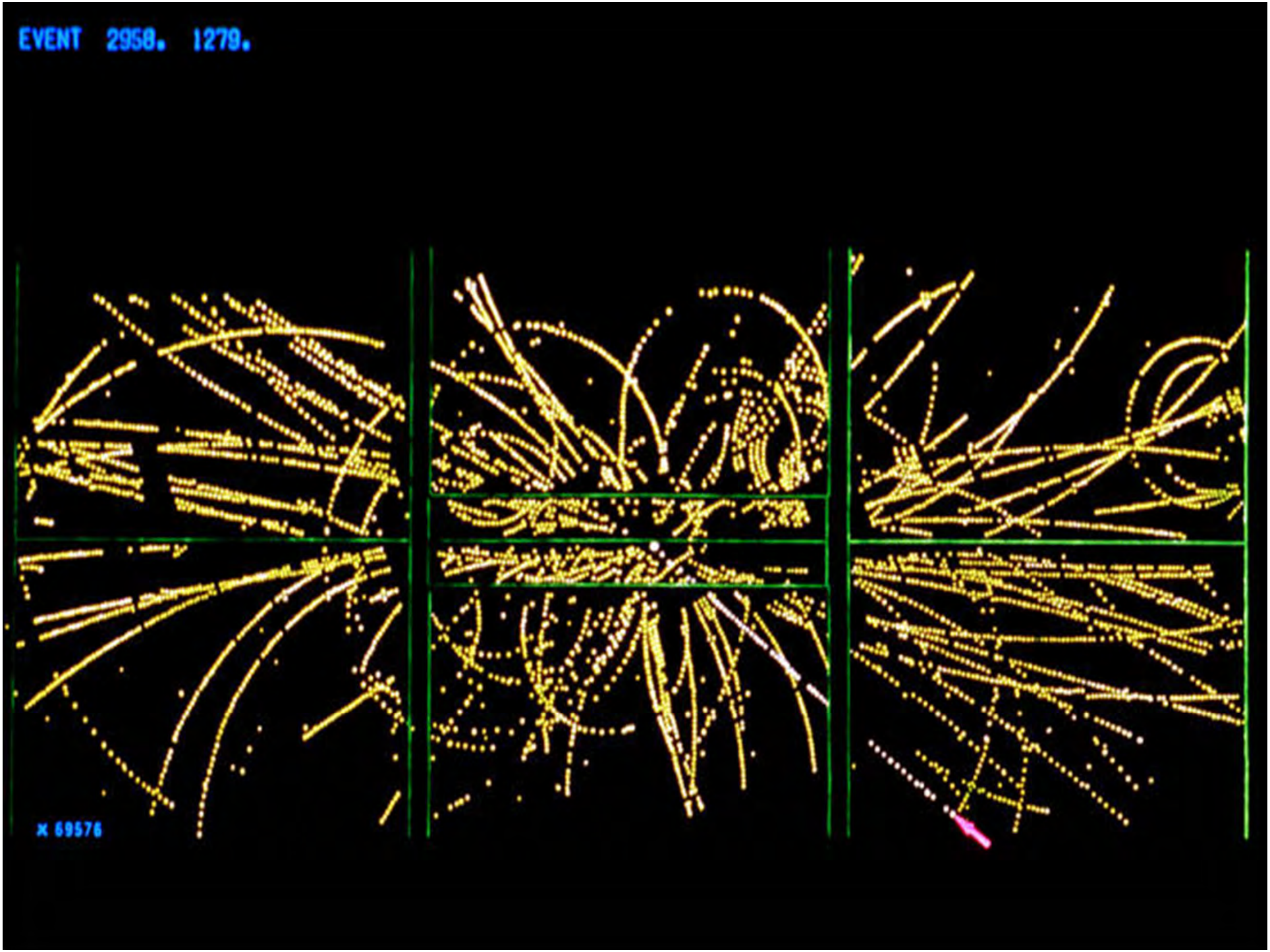
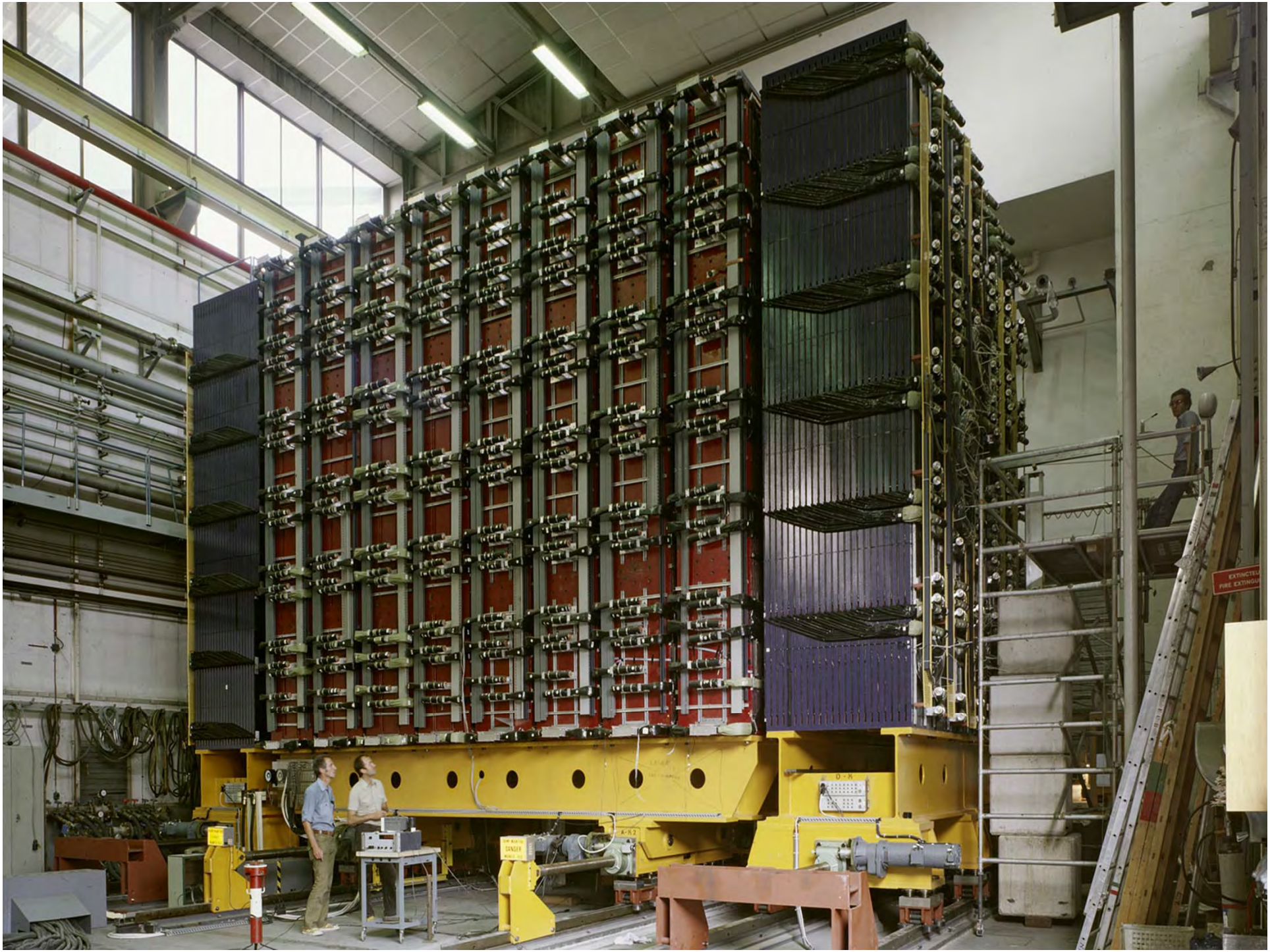
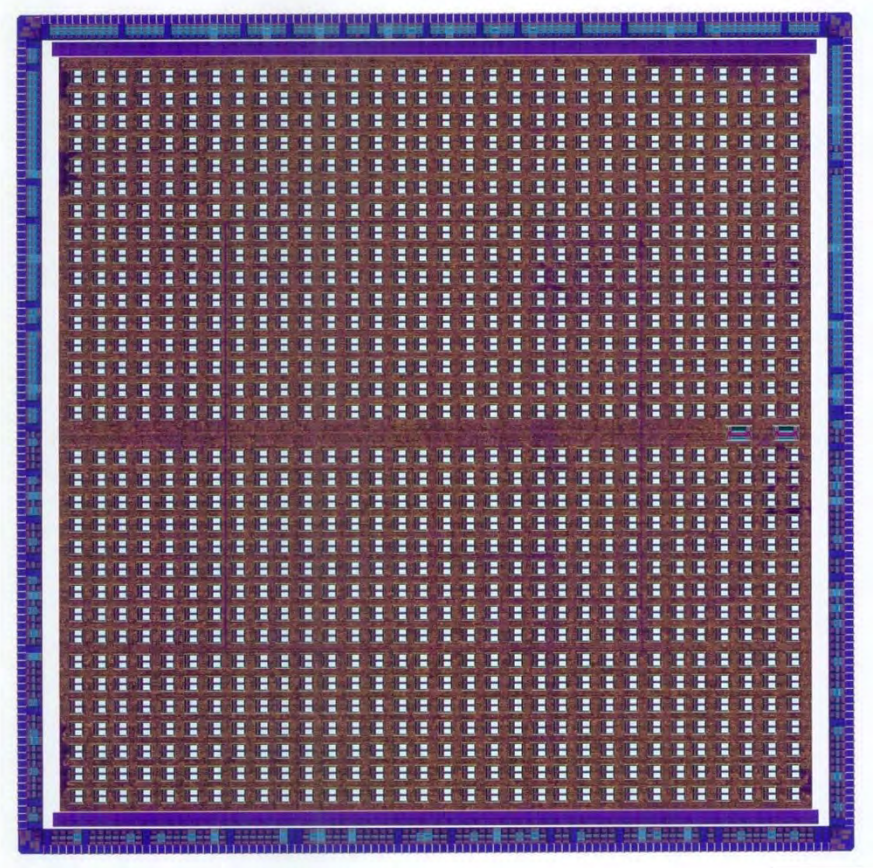

EVENT 2958. 1279.
X 69576


DANGER



NEUROMEM DIGITAL PATTERN RECOGNITION AND LEARNING CHIP

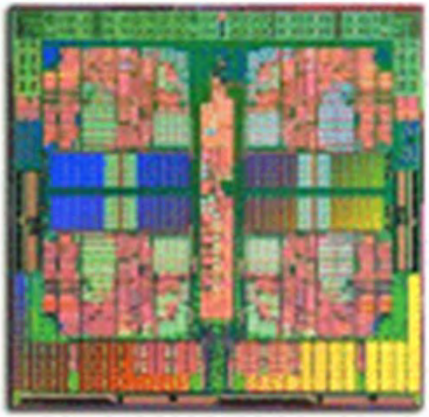
NATIVELY PARALLEL ARCHITECTURE WITH NO INSTRUCTION SET

Hardware Aspects of the Cortical Processor
Workshop September 18-19 2013

The NeuroMem computing alternative

Common platforms

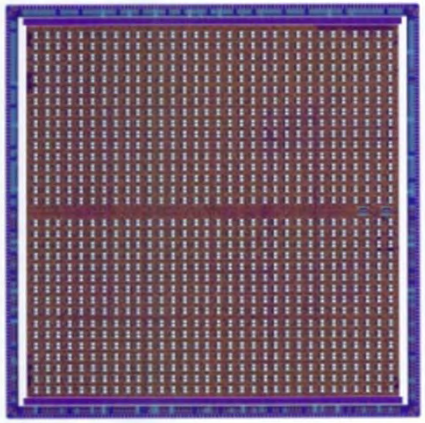
A multicore processor surrounded by DMA and SDRAM controllers; >1 GHz, >10 W



- Multi-core processors
- Memory misery bottleneck
- Limited by the Amdahl's law
- High frequencies (GHz), Power demanding (10W)
- Complex programming

NeuroMem

Neuromorphic memory with 1024 identical cells; <16 Mhz, <0.5 W



- Memory and processing logic combined in a same cell
- Identical cells working in parallel
- Fixed number of I/Os independent of the number of cells
- Zero Instruction Set Computing architecture
- less than 1 M$ development cost
- 130 nm 8 Metal layers 8x8 mm dies size

The 8 pillars of neuromorphic Pantheon

- **Broadcast Mode :** query/stimulus is broadcasted to all the neurons of a "context group" simultaneously
- **Deterministic search time:** does not increase with the scaling up of the network
- **Winner takes all:** Inhibit the weak responders autonomously in the same deterministic time
- **Uncertain response:** when there is multiple/conflicting neurons responding or "lesser quality" (degenerated) neurons spiking.
- **Unknown response:** Enable the dynamic addition of new knowledge
- **Back propagation of error:** Self & parallel inhibition of erroneous spiking neurons, no software involved
- **No fetch and decode of program instruction:** Software is definitively contrary to the biological model, else it's simulation, not neuromorphic…
- **Beyond biology:** Fast upload download enabling knowledge proliferation (some dream of it).

Merger of 2 concepts

Non-linear classifier

***1974**, Compound classifier invented by Bruce Batchelor*

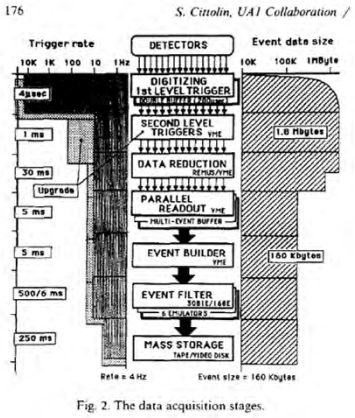
***1982** - Restricted Coulomb Energy classifier, derived by Leon Cooper (Nobel prize for supraconductivity)*

Hardwired parallel architecture

***1984** - CERN's UA1 experiment lead by Nobel prize winner Carlo Rubbia*

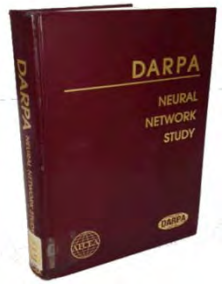
Guy Paillet DataSud Systems design a parallel architecture (60 CPU's/Memory on same VME bus)

Big Data before time (250 GB/sec)



***1988** – DARPA Neural Network Study*

"The technology is not mature for widespread practical applications, since computer simulation are the primary methods of implementation."



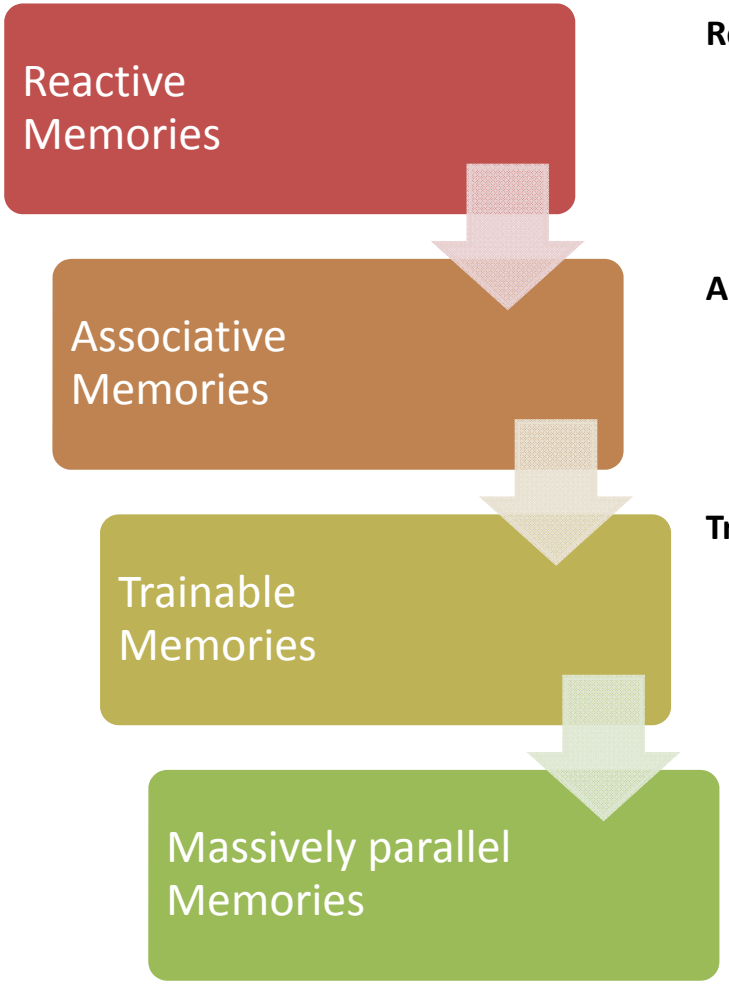
***1993** - ZISC (Zero Instruction Set Computer with 36 and later 78 neurons)*

designed by IBM France and Guy Paillet

***2009** - CM1K (Cognitive Memory with 1024 neurons)*

designed by Anne Menendez and Guy Paillet

The NeuroMem Innovation



Reactive Memories

Deliver answers voluntarily when an input data matches their content. Instead of having a CPU screen sequentially what every memory 'knows', the memories volunteer their response in an orderly manner.

Associative Memories

React not only when an input data matches their content, but also when it is similar "enough". This feature extends the usage model to a **non linear classifier.**

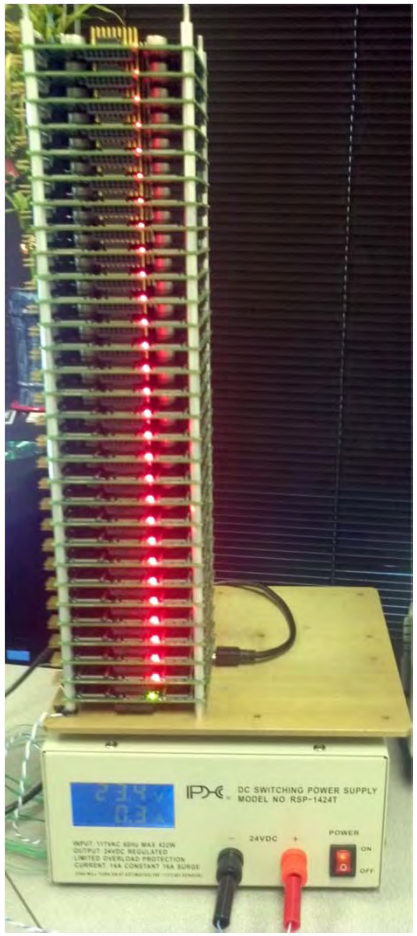
Trainable memories

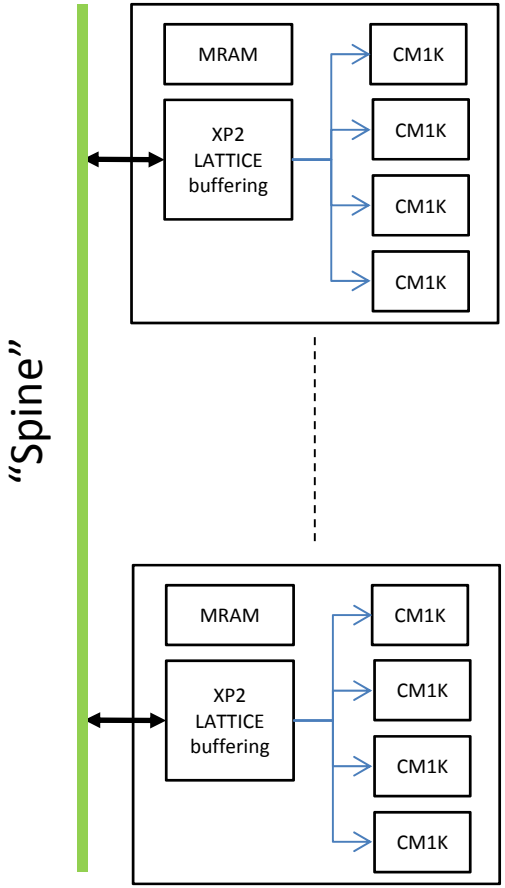
Know when an input data represents novelty. Can learn/add new models in real-time. If applicable, the memory cells recognizing the new example erroneously correct their influence field autonomously . This feature extends the usage model to a **trainable neural network.**

Massively parallel memories

Implement a natively parallel architecture which allows the sizing of any bank of cognitive memories WITHOUT impacting the I/O counts nor the existing interfaces to external hosts. The memories connected in parallel are operated at low frequency and therefore require low-power.

A stack of 100,000 neurons fully operational



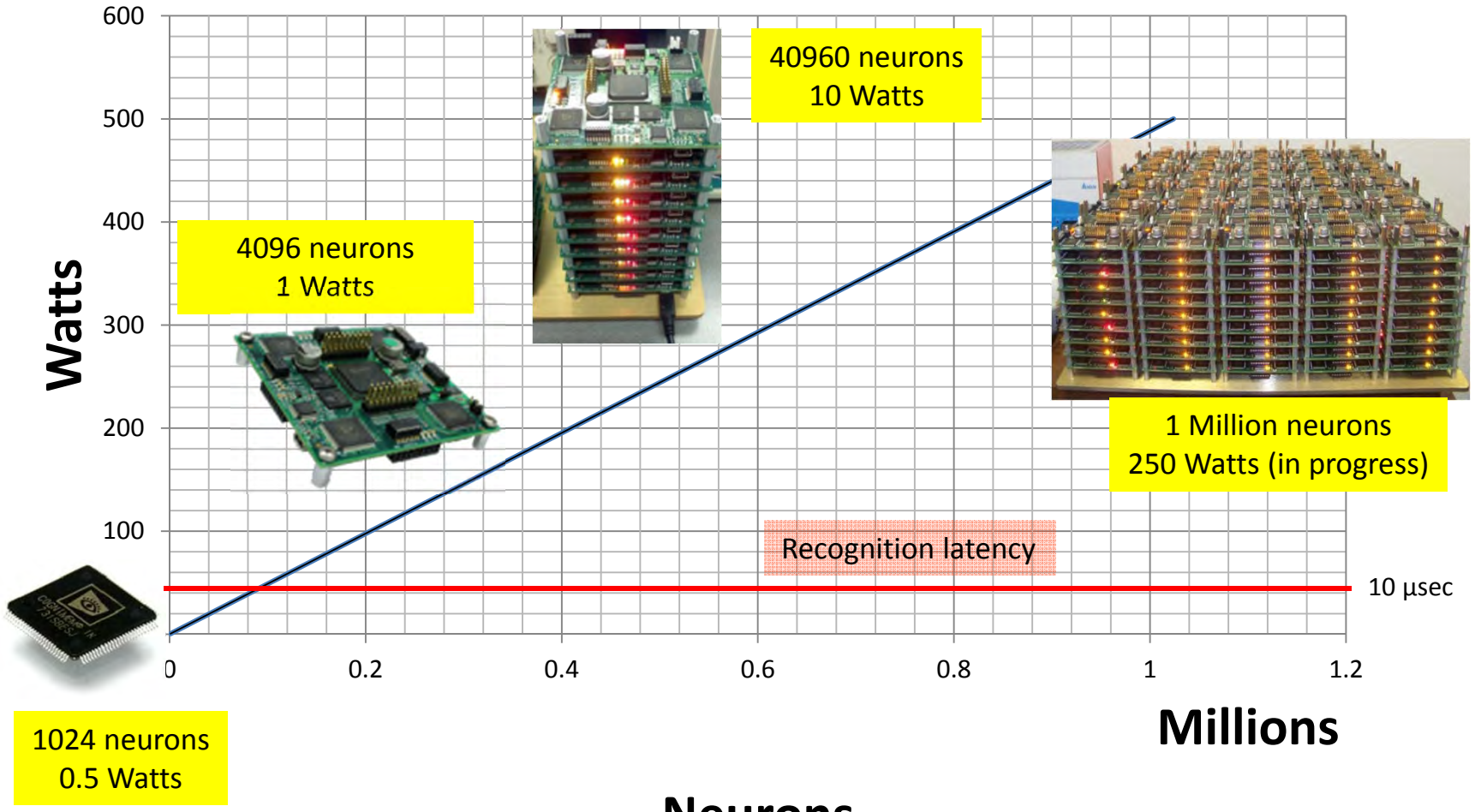


UP TO 25 NeuroMem Boards
409,600 operations per clock cycle @ 10 MHz
Total ~4 Tera Ops/sec
25 Watts

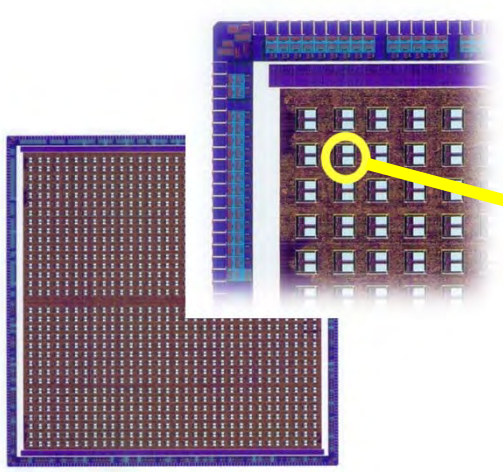
NEXT STEP

Reduce to a single chip of 100,000 neurons in 2014 (28 nm, 6x6 mm^2)

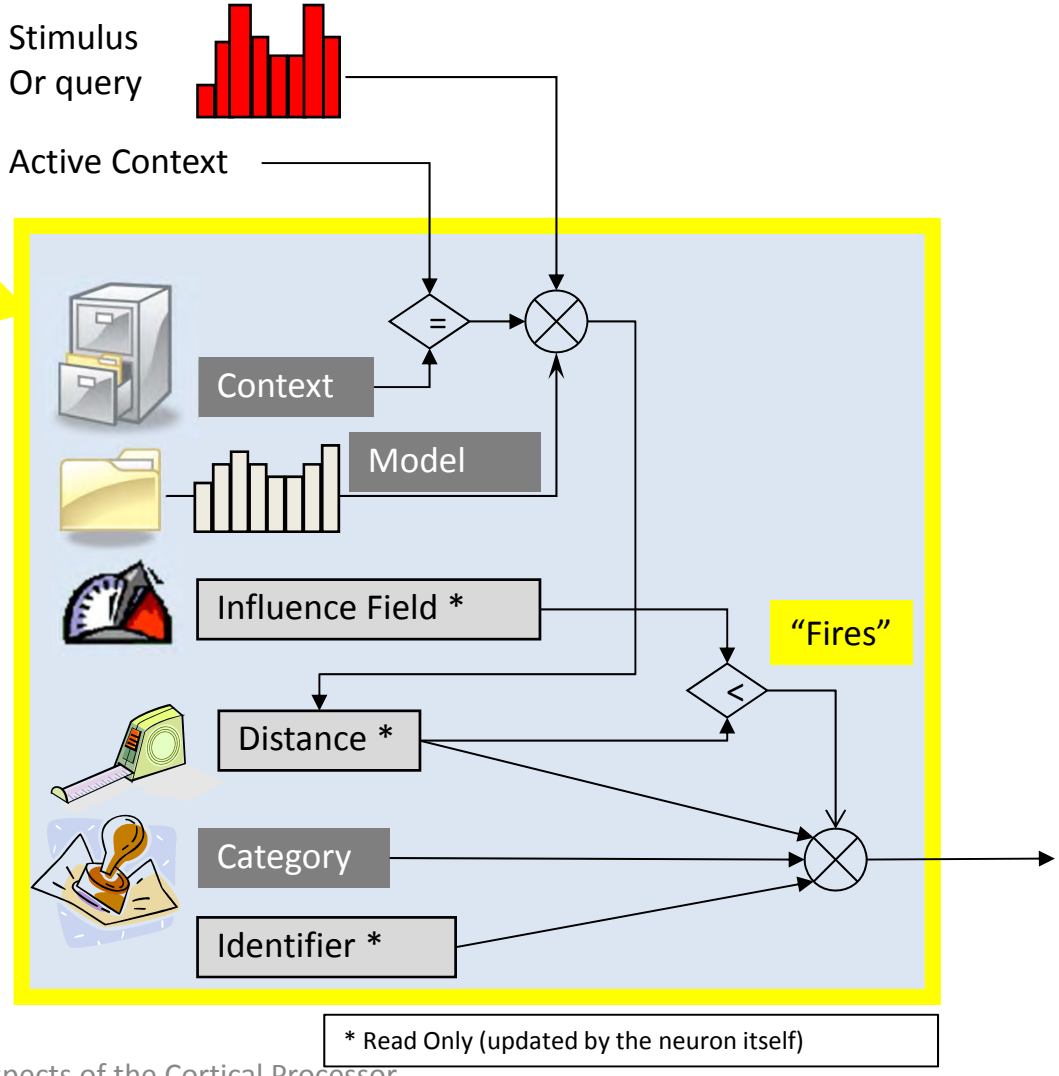
Demonstrated high Scalability



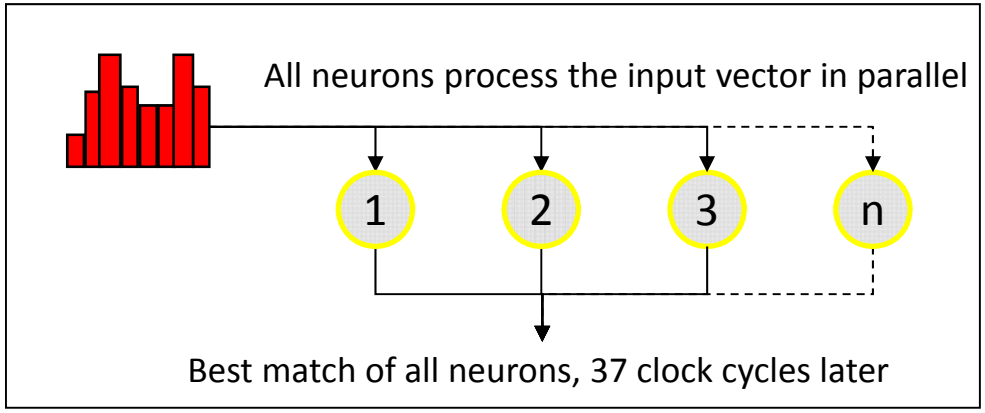
CM1K neuron



A CM1K neuron react (spike) which when incoming pattern is “similar” to its “learned” a memory. Similarity domain is adapted by excitation/inhibition during the teaching process. CM1K neurons are also able to make unsupervised leaning (e.g. clustering, etc…)

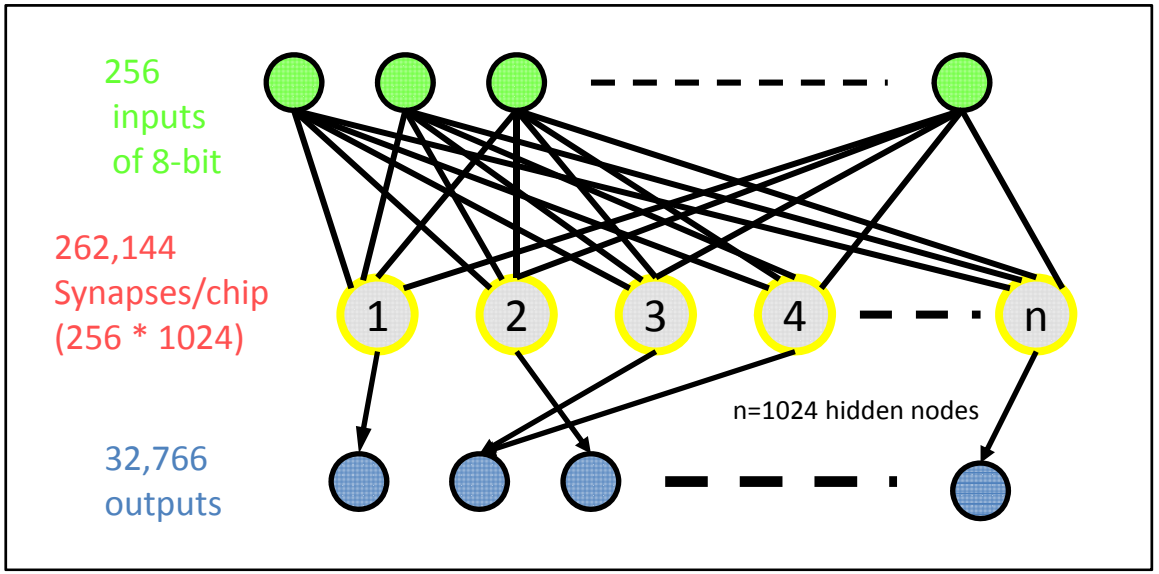


CM1K network



A neural network is a bank of neurons operating in parallel and interacting together to learn autonomously and recognize so that the **winner-takes-all**. All neurons have the same behavior and execute the instructions in parallel with no need for a controller or supervisor

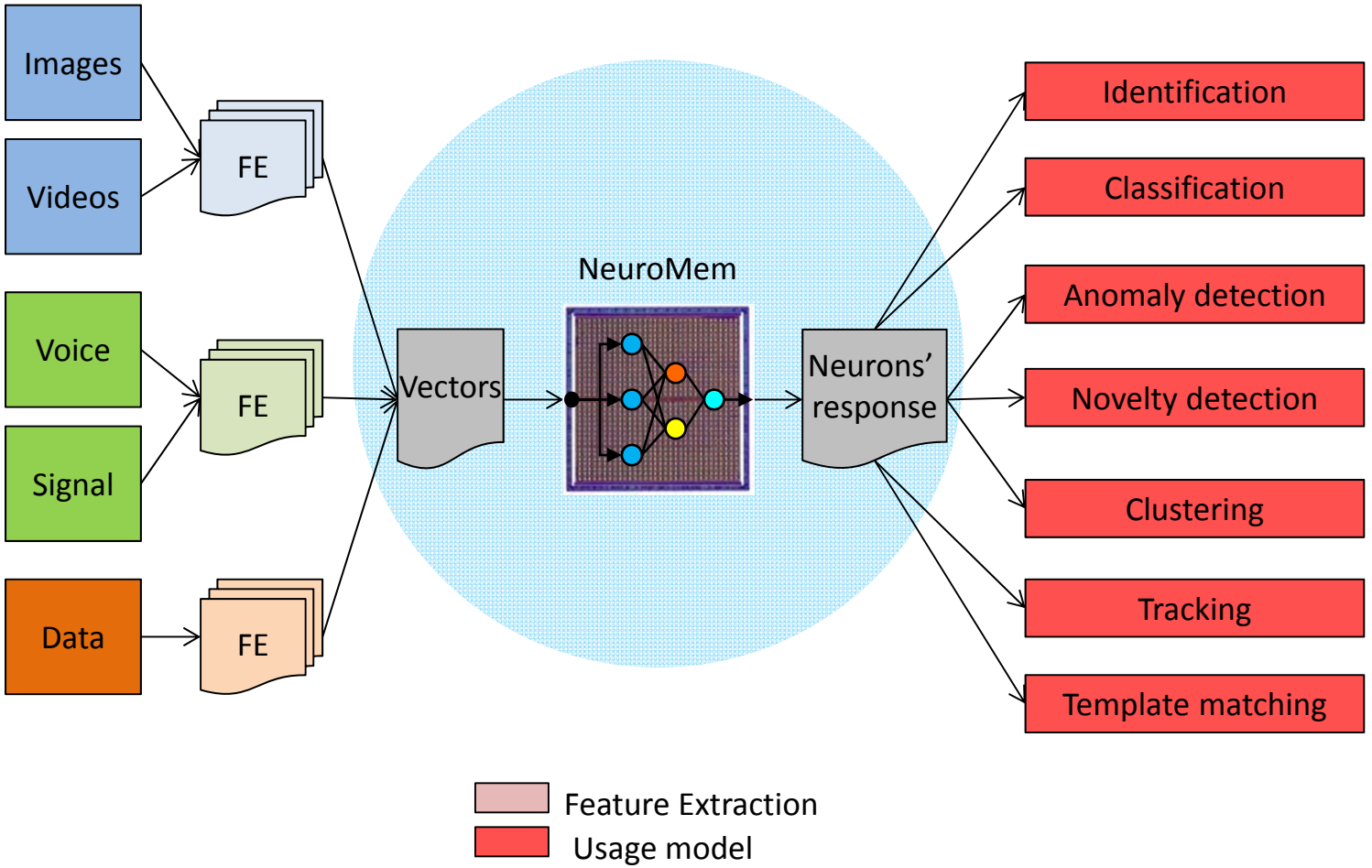
CM1K seen as a 3-layer network



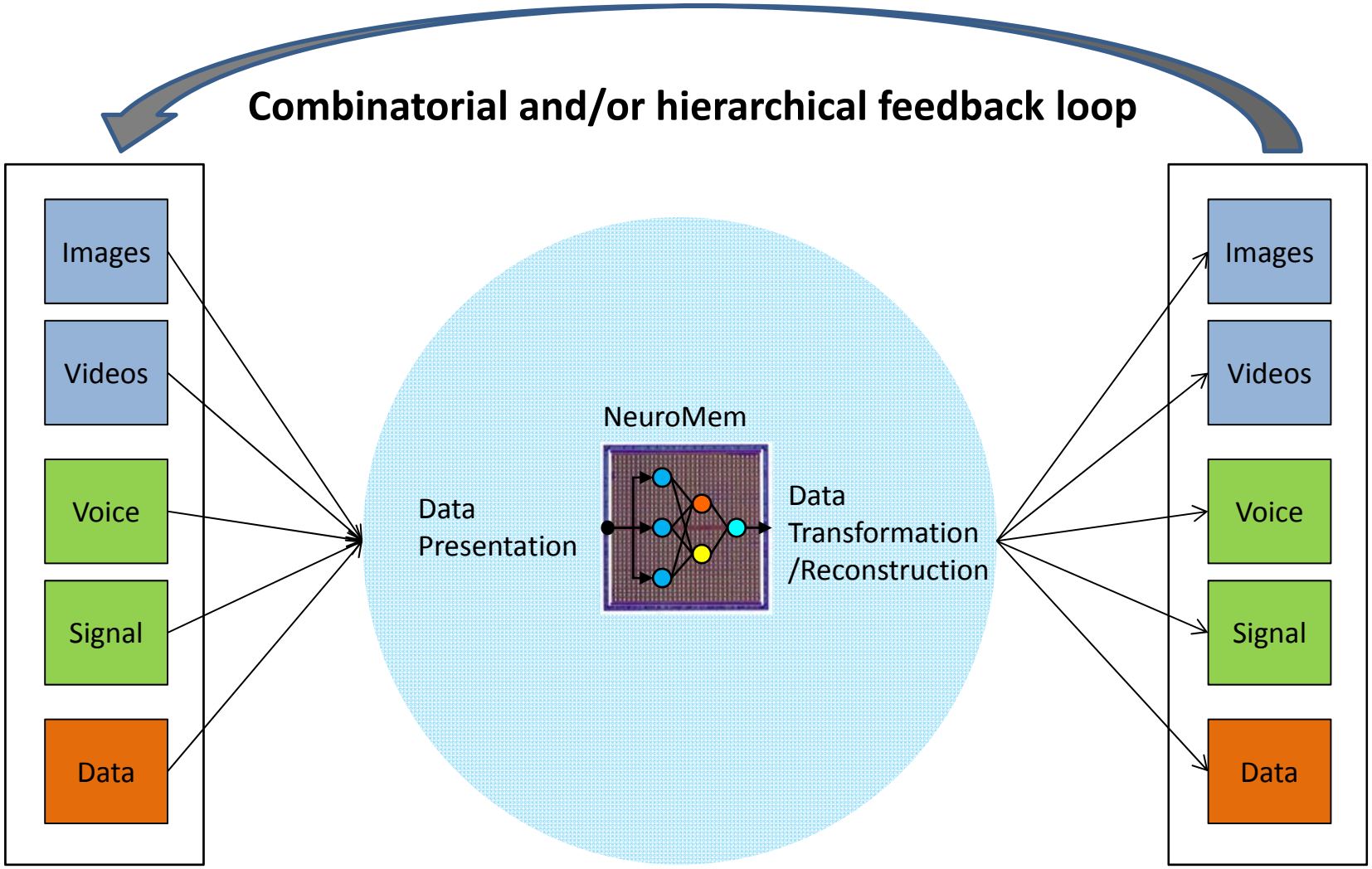
Functions performed:

- o Identification
- o Classification
- o Clustering
- o Anomaly Detection
- o Novelty Detection

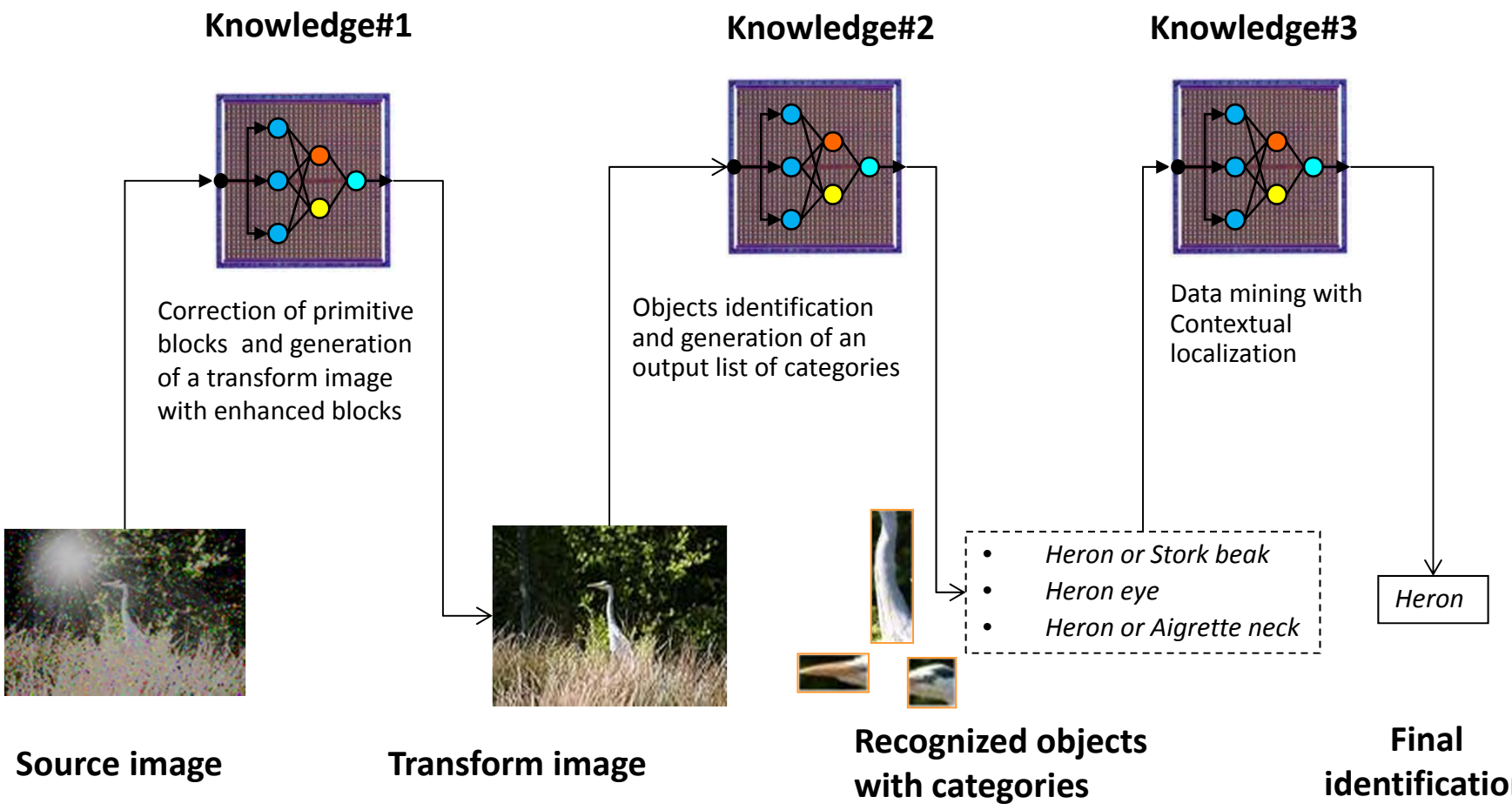
Usage Models, Level1



Usage Models, Level2



Ex1: Hierarchical decision making

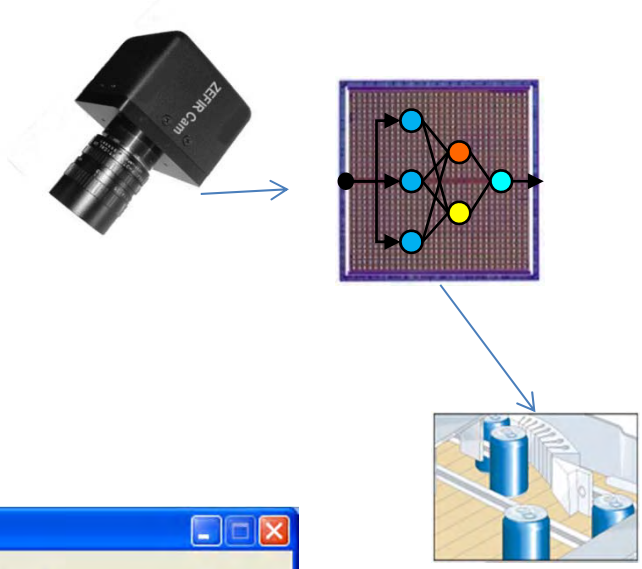


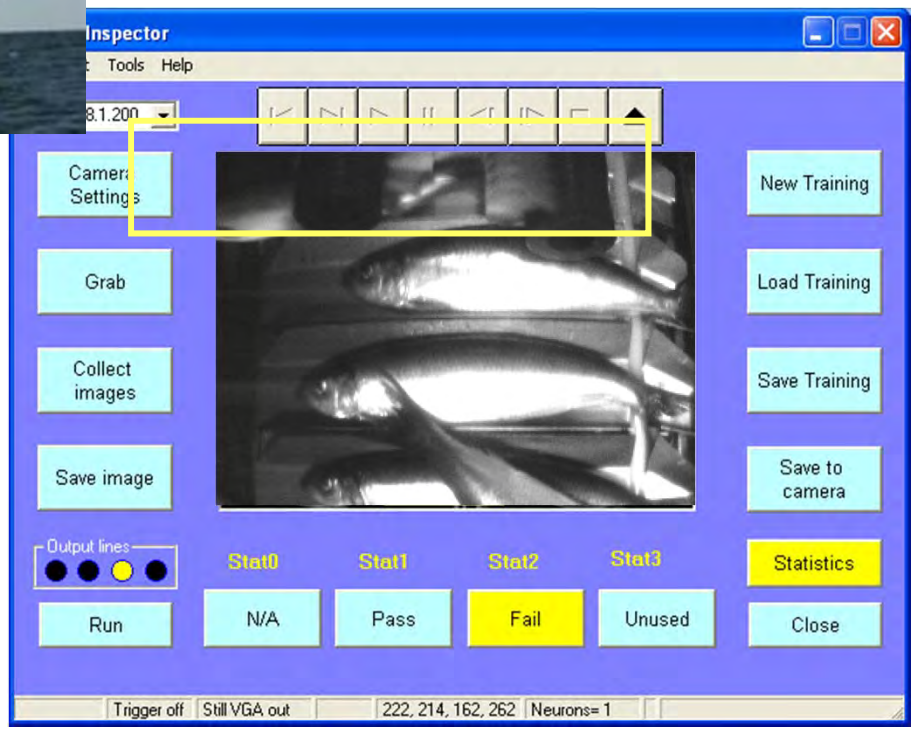
Applications

Cognitive storage	• In storage search engines , scalable content access memory banks, intrinsic de-duplication, no need for indexing
Cognitive Sensing	• Convert sensor signals into insight data at the source and in real-time, selective transmission
Cognitive networking	• Match content of high speed data stream in real-time, selective pull data forward or exclusion

A companion chip to off-load Van Neumann machines from pattern recognition tasks

Fish Inspection





Pisces.wmv

Adaptive Optics

A MINIATURISED WAVEFRONT SENSOR BASED ON A SILICON NEURAL NETWORK
(High-speed Function Approximation)

01/03/2010 – 31/08/2010

Robotics

RoadNarrows Robotics
ROBOTICS AND INTELLIGENT SYSTEMS

CogniBoost™

CogniBoost™ offers an affordable, low-power, fast, pattern recognition module ideal for control applications, robotics, vision, & data mining.

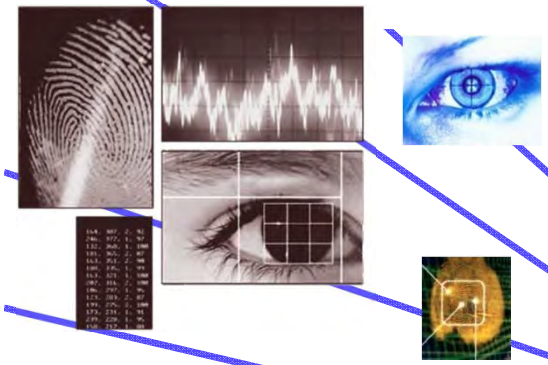
Features:

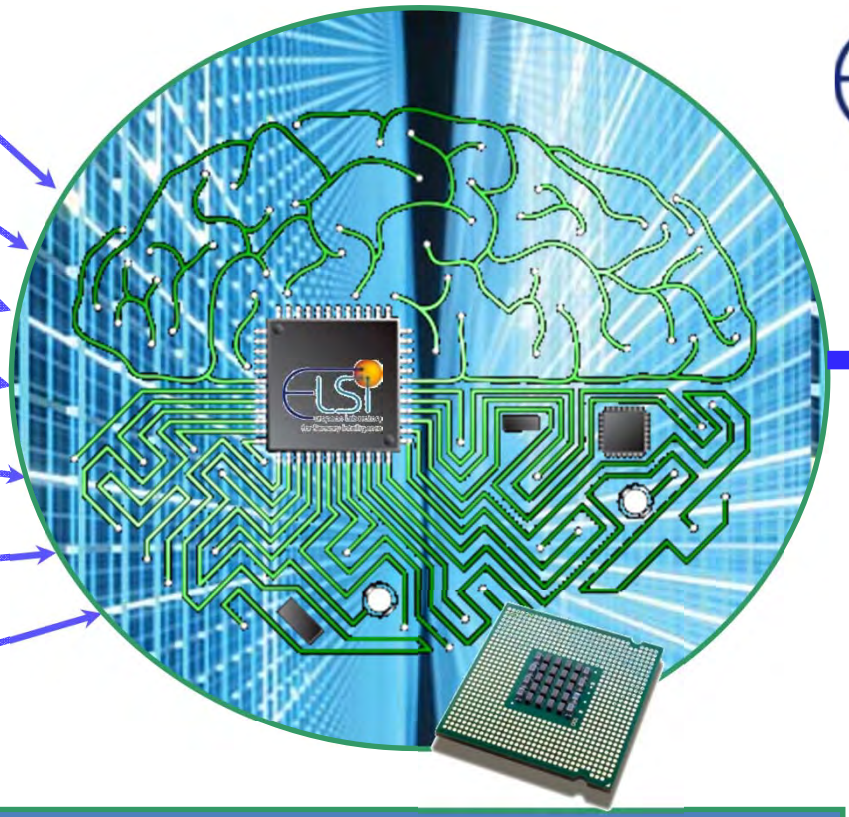
- Powerful embedded NeuroMem chip.
- USB interface provides both power and data interface to host.
- Standard USB driver support for Linux, Windows (FTDI) for USB to Serial COM.
- On-board non-volatile memory to store trained pattern categories & configuration.
- Binary or ASCII communications mode for different applications.
- Simple Microchip PIC managing protocol, neuron storage, and communications.
- Open protocol, free source code, & python examples for host applications.
- Supported by RoboRealm™ software under Windows.
- Ideal for embedded applications.

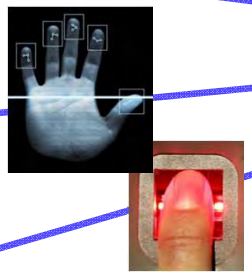
www.roadnarrows-store.com/products/think/cognitive-systems.html

Big Artificial Brain

Artificial Intelligence and true parallel computing embedded system
for ultra fast data base analysis by pattern matching







Biometric Data
DNA – fingerprint – iris – voice

Identification

Goal : 10^6 decision cells in parallel

Droppable and disposable Miniature Visual Event Detector (in progress)

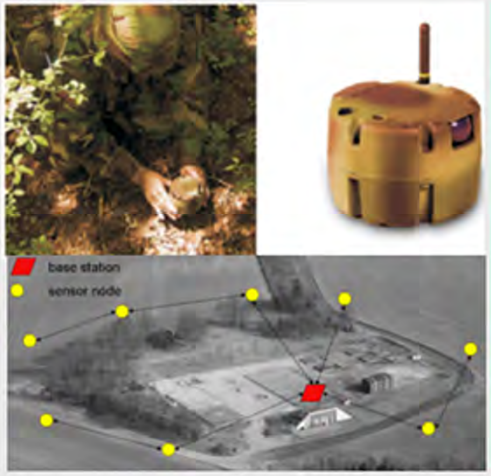
ATC/ELSI Team

ELSI European Laboratory for Sensory Intelligence

MVED : Miniature Visual Event Detector
GENERIC USE CASES 2/3

AI on silicon could increase the performances of the sensors and the safety of our troupes, patrols, infrastructures.

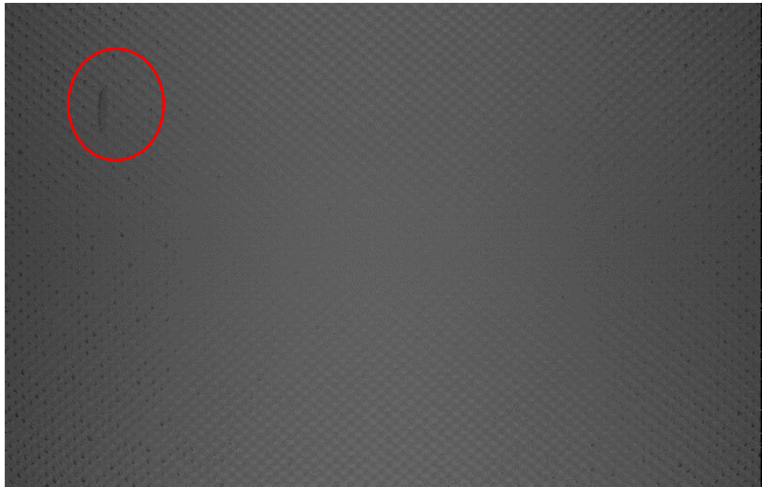
➢Increasing the number of MVED virtual experts

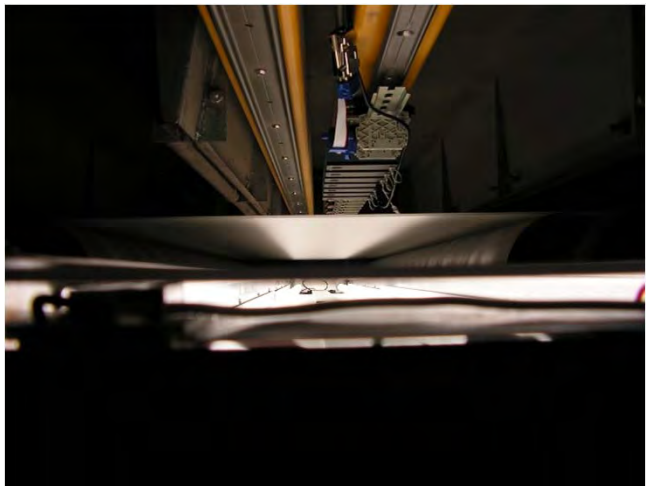


- An intelligent camera could learn and track automatically a designed vehicle from node to node.
- The knowledge: a car signature … could be transferred to the other cameras at different sensitive points of the town.
- An intelligent camera could be trained to recognize ambulances and or vehicles of friendly forces.

8/14

Surface Anomaly Detection





The ZISC architecture timeline

1969-74 Bruce G. Batchelor publishes his landmark book

Batchelor, B. G. 1969. Learning Machines for Pattern Recognition. Ph.D. thesis, University of Southampton, Southampton, England.

Batchelor, B. G. 1974. *Practical Approach to Pattern Classification.* New York: Plenum.

Batchelor, B. G. 1978. Classification and Data Analysis in Vector Space. In *Pattern Recognition*, ed. B. G. Batchelor, pp. 67–116. London: Plenum.

1982 Leon N. Cooper and all, derived a digital architecture (RCE) founded NESTOR but finally resort to software implementation

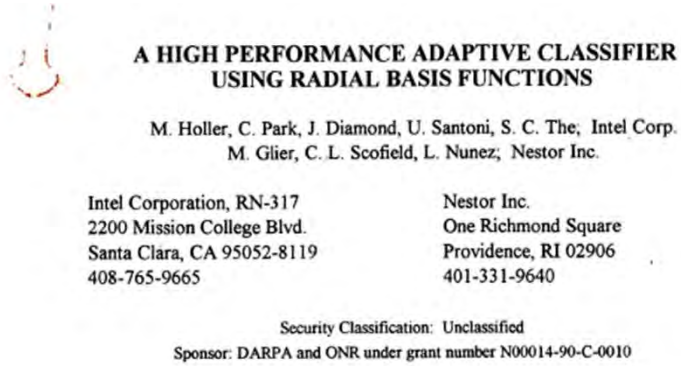
Reilly, D. L., L. N. Cooper, and C. Elbaum. 1982. A Neural Model for Category Learning. *Biol. Cybernet.* 45:35–41.

Reilly, D. L., C. Scofield, C. Elbaum, and L. N. Cooper. 1987. Learning System Architectures Composed of Multiple Learning Modules. *Proc. IEEE First International Conference on Neural Networks*, San Diego, June 21–24.

The ZISC architecture timeline

1990 Nestor and Dassault Aircraft starts Nestor Europe with Guy Paillet as CEO

1992 Nestor US starts a contract with DARPA and Intel for the NI1000



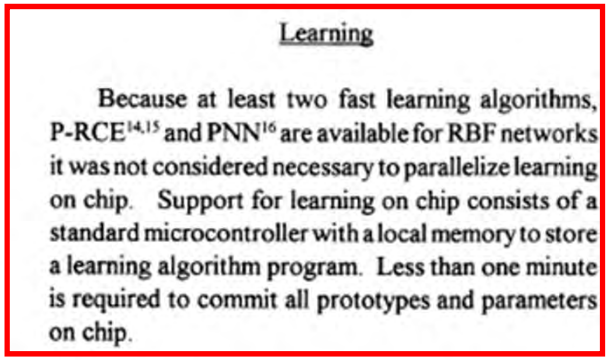
A HIGH PERFORMANCE ADAPTIVE CLASSIFIER USING RADIAL BASIS FUNCTIONS

M. Holler, C. Park, J. Diamond, U. Santoni, S. C. The; Intel Corp.
M. Glier, C. L. Scofield, L. Nunez; Nestor Inc.

Intel Corporation, RN-317
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
408-765-9665

Nestor Inc.
One Richmond Square
Providence, RI 02906
401-331-9640

Security Classification: Unclassified
Sponsor: DARPA and ONR under grant number N00014-90-C-0010



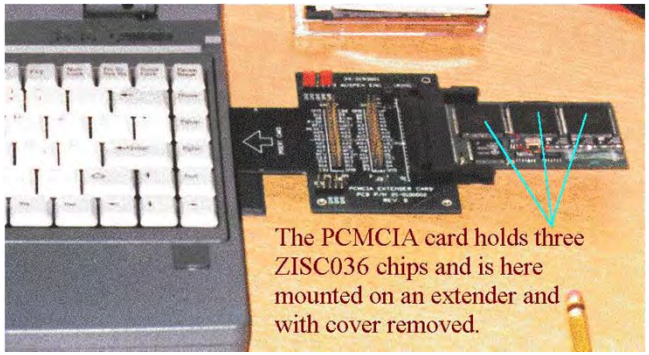
Learning

Because at least two fast learning algorithms, P-RCE[14,15] and PNN[16] are available for RBF networks it was not considered necessary to parallelize learning on chip. Support for learning on chip consists of a standard microcontroller with a local memory to store a learning algorithm program. Less than one minute is required to commit all prototypes and parameters on chip.

1992 Guy Paillet leaves Nestor Europe and establish NeurOptics in Montpellier France. He brought the ZISC concept in 1993 to IBM France and develop jointly the ZISC36 as an independent partner

The ZISC architecture timeline

1993 partnership between
IBM France and NeurOptics resulted in 5 international patents owned jointly by IBM/Guy Paillet for Zero Instruction Set Computer architecture and in the ZISC36 (36 neurons)
Design of a PCMCIA board for French Defense (108 neurons)



Courtesy of Royal Institute of Technology Stockholm Sweden

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 694 852 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
26.06.2002 Bulletin 2002/26

(51) Int Cl.[7]: **G06F 15/80**, G06K 9/66

(21) Application number: **94480067.1**

(22) Date of filing: **28.07.1994**

(54) **Innovative neuron circuit architectures**

Innovative Neuronalschaltungsarchitektur

Architectures de circuit neuronal innovatrices

(84) Designated Contracting States:
DE FR GB

(43) Date of publication of application:
31.01.1996 Bulletin 1996/05

(73) Proprietors:
- **International Business Machines Corporation**
  Armonk, N.Y. 10504 (US)
- **Paillet, Guy**
  34000 Montpellier (FR)

(72) Inventors:
- **Boulet, Jean Yves**
  F-91610 Ballancourt Sur Essonne (FR)
- **Godefroy, Catherine**
  F-91100 Corbeil Essonnes (FR)
- **Steimle, André**
  F-91000 Evry (FR)
- **Louis, Didier**
  F-77300 Fontainebleau (FR)
- **Paillet, Guy**
  F-3400 Montpellier (FR)
- **Tannhof, Pascal**
  F-77930 Cely en Bière (FR)

(74) Representative: **Klein, Daniel Jacques Henri**
Compagnie IBM France
Département de Propriété Intellectuelle
06610 La Gaude (FR)

(56) References cited:
EP-A- 0 295 876 **US-A- 5 239 594**

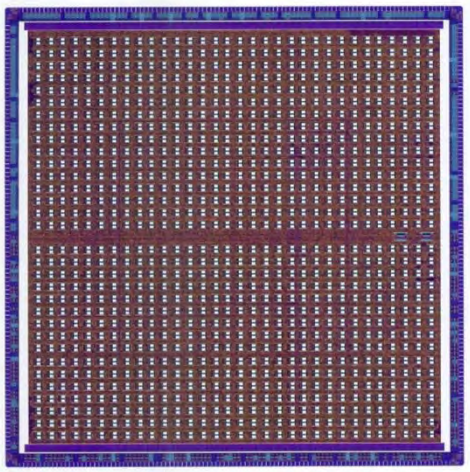
- **IJCNN INTERNATIONAL JOINT CONFERENCE ON NEURAL NETWORKS, vol.4, 7 June 1992, BALTIMORE , USA pages 228 - 234 IWATA 'Hand-written alpha-numeric recognition by a self-growing neural network "combNET-II"'**

The ZISC architecture timeline

- 1993-1996 NeurOptics is consulting for DGA GIAT Industries (French Defense)
- 1999 GP joins Anne Menendez in Petaluma CA to work on “generic vision”
- 2006 General Vision start the CogniMem chip CM1K with funding from angels investors
- 2007 CM1K is released into production at OKI Semiconductor
- 2013 CogniMem is renamed NeuroMem

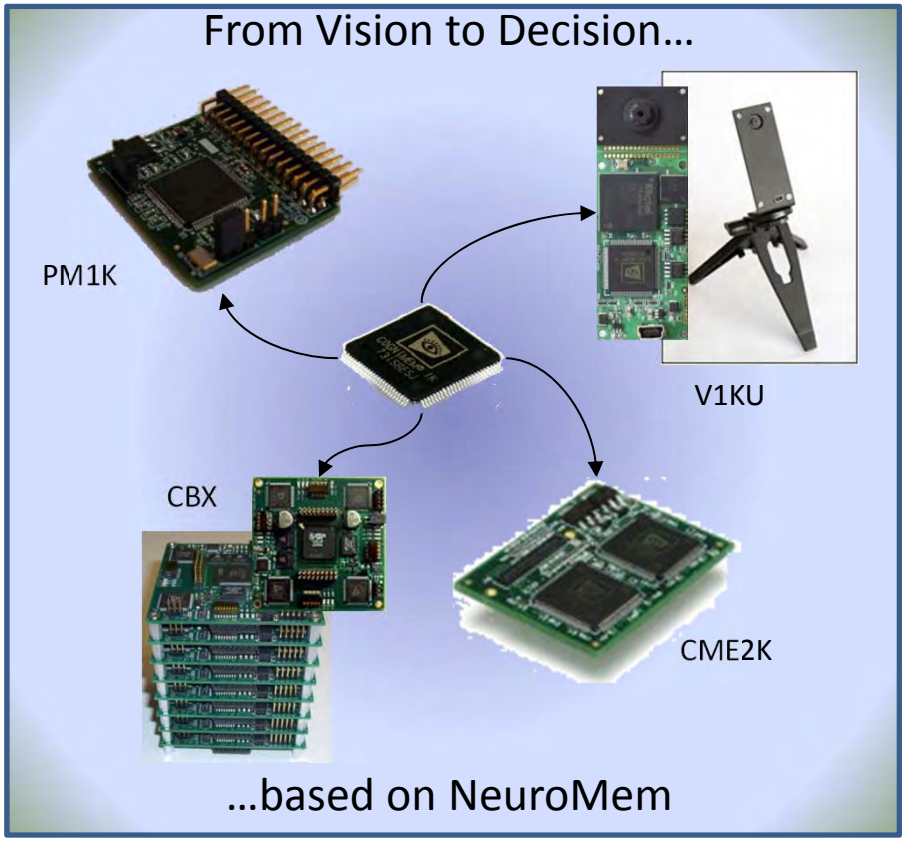
2007, here comes CogniMem now NeuroMem®

- General Vision (Anne Menendez and GP) develops the CM1K with OKI being chosen as foundry subcontractor
- At the same time General Vision is developing a glass inspection system for Asahi Glass and applying the “IntelliGlass” patent (now granted)



Evaluation products & Licensing

- Sensing platforms
  - PM1K with I2C bus
  - V1KU with CMOS sensor
  - CBX with I/Os for sensors
- Computing platforms
  - CBX, stackable
  - CME2K
- Software tools
  - C++, C#, MatLab API
  - Image Knowledge Builder
- Training classes
- FPGA IP and ASUIC IP licensing



- For product information, visit www.general-vision.com